AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A bit synchronizing circuit used for a reception circuit for serial communication, comprising:

a polyphase clock generation circuit for generating a plurality of clocks which are out of phase with each other by a regular interval, based on an input clock, the polyphase clock generation circuit including a plurality of delay circuits connected in series and one of said plurality of delay circuits delaying the input clock;

a detection circuit for detecting which clock has a phase shift of an integral multiple of a clock cycle among the clocks generated by the polyphase clock generation circuit with respect to the clock generated by the delay circuit that delays the input clock ~~one of said plurality of generated clocks~~; and

a clock selecting circuit to which a polyphase clock is inputted from the polyphase clock generation circuit and which selects an outputted polyphase clock based on a detection result from the detection circuit.

2. (Original) The bit synchronizing circuit of claim 1, wherein the polyphase clock generation circuit is formed by connecting a plurality of delay circuits which delay the input clock by almost the same amount of time.

3. (Previously Presented) A bit synchronizing circuit for a reception circuit for serial communication, comprising:

a polyphase clock generation circuit for generating a plurality of clocks which are out of phase with each other by a regular interval, based on an input clock;

a detection circuit for detecting which clock has a phase shift of an integral multiple of a clock cycle among the clocks generated by the polyphase clock generation circuit with respect to the input clock;

a logic circuit to which an output from the detection circuit is inputted; and

a latch circuit to which an output from the logic circuit is inputted and of which an output is inputted to the logic circuit.

4. (Original) The bit synchronizing circuit of claim 3, wherein the data of the latch circuit is cleared with a constant timing.

5. (Currently Amended) A bit synchronizing circuit used for a reception circuit for serial communication, comprising:

a polyphase clock generation circuit for generating a plurality of clocks which are out of phase with each other by a regular interval, based on an input clock, the polyphase clock generation circuit including a plurality of delay circuits connected in series and one of said plurality of delay circuits delaying the input clock;

a detection circuit for detecting which clock has a phase shift of an integral multiple of a clock cycle among the clocks generated by the polyphase clock generation circuit with respect to the clock generated by the delay circuit that delays the input clock ~~one of said plurality of generated clocks~~; and

an operational circuit for sampling an output from the detection circuit a plurality of times and carrying out an operation on the plurality of sampled values.

6. (Previously Presented) The bit synchronizing circuit of claim 3, wherein an output from the detection circuit is held for a constant cycle time and is updated at each constant time unit.

7. (Original) The bit synchronizing circuit of claim 6, wherein the output from the detection circuit is held at the time of bit data reception.

8. (Currently Amended) A bit synchronizing circuit used for a reception circuit for serial communication, comprising:

a polyphase clock generation circuit for generating a plurality of clocks which are out of phase with each other by a regular interval, based on an input clock, the polyphase clock generation circuit including a plurality of delay circuits connected in series and one of said plurality of delay circuits delaying the input clock;

a detection circuit for detecting which clock has a phase shift of an integral multiple of a clock cycle among the clocks generated by the polyphase clock generation circuit with respect to

the clock generated by the delay circuit that delays the input clock ~~one of said plurality of generated clocks~~;

a plurality of bit synchronous working circuits to which a polyphase clock is inputted from the polyphase clock generation circuit so that a bit synchronizing operation is carried out at each different phase; and

a selecting circuit for selecting outputs from the plurality of bit synchronous working circuits, based on the detection result of the detection circuit.

9. (Previously Presented) The bit synchronizing circuit of claim 3, comprising:

a clock selecting circuit to which a polyphase clock is inputted from the polyphase clock generation circuit and which selects an outputted polyphase clock based on a detection result from the detection circuit.

10. (Previously Presented) The bit synchronizing circuit of claim 5, wherein an output from the detection circuit is held for a constant cycle time and is updated at each constant time unit.

11. (Previously Presented) The bit synchronizing circuit of claim 5, comprising:

a clock selecting circuit to which a polyphase clock is inputted from the polyphase clock generation circuit and which selects an outputted polyphase clock based on a detection result from the detection circuit.

12. (Previously Presented) The bit synchronizing circuit of claim 3, wherein the polyphase clock generation circuit is formed by connecting a plurality of delay circuits which delay the input clock by almost the same amount of time.

13. (Previously Presented) The bit synchronizing circuit of claim 5, wherein the polyphase clock generation circuit is formed by connecting a plurality of delay circuits which delay the input clock by almost the same amount of time.

14. (Previously Presented) The bit synchronizing circuit of claim 8, wherein the polyphase clock generation circuit is formed by connecting a plurality of delay circuits which delay the input clock by almost the same amount of time.

15. (Previously Amended) The bit synchronization circuit of claim 1, wherein said detection circuit comprises a plurality of flip-flops, each flip-flop having an input for said one of said plurality of generated clocks and an input for a respective clock among the clocks generated by the polyphase clock generation circuit.